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10/743,165	12/22/2003	Norbert R. Seifert	200209635-1	7761

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EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/743,165	SEIFERT ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/22/03, 12/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed December 22, 2003, the Information Disclosure Statement filed December 22, 2003, the Information Disclosure Statement filed December 14, 2005.

2. Claims 1-22 are pending in the case. Claims 1, 10, 16, and 20 are independent claims.

Information Disclosure Statement

3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on December 22, 2003 and December 14, 2005. These IDS have been considered.

Specification

4. The abstract of the disclosure is objected to because: legalese and statements which may be implied.

In the Abstract, lines 1-2, it is suggested to change "reducing soft errors is disclosed. In some embodiments the method comprises: assigning" to --reducing soft errors in which the method includes: assigning--.

Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 15 is objected to because of the following informalities: antecedent basis.

In Claim 15, it is suggested to change "the timing signal" to --a timing signal--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 10, 11, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Madden et al. (U.S. Patent 4,910,713).**

Regarding independent claim 10, Madden et al. show a storage circuit (Fig. 1) comprising:

a plurality of nodes (Fig. 1: 26, 24) including a first node (Fig. 1: 26) and a second node (Fig. 1: 24), wherein the second node is coupled to the first node;

a plurality of signals (Fig. 1: 12, 14, and 28) coupled to the storage circuit, wherein the signals enable a first node to change (see Fig. 3: time t3, 20 which is connected to node 26 changes from Vdd to Vss) from a predetermined state (Vdd); and

a circuit element (Fig. 1: P3) coupled to the second node, wherein the circuit element maintains (see Fig. 3: at time t3, 22 which is node 24 maintains Vdd) the second node in its predetermined state (Vdd) for a predetermined period of time.

Regarding dependent claim 11, Madden et al. show the circuit element further comprises metal oxide semiconductor field effect transistors ("MOSFETs") (see Fig. 1: P3 is a MOS transistor).

Regarding dependent claim 13, Madden et al. show an inverter (Fig. 1: P2 and N1 form an inverted coupled between node 24 and node 26; and P3 and N2 form an inverter coupled between node 26 and node 24) is coupled between the first node and the second node.

Regarding dependent claim 14, Madden et al. show a plurality of inverters (Fig. 1: P2 and N1 form an inverted coupled between node 24 and node 26; and P3 and N2 form an inverter coupled between node 26 and node 24) coupled between the first and second nodes.

Regarding dependent claim 15, Madden et al. show a timing signal (Fig. 1: AMP STROBE) comprises a pre-charge phase (see Fig. 3: AMP STROBE at t1 and t2) and an evaluate phase (see Fig. 3: AMP STROBE at t3), and wherein the nodes are set high during the pre-charge phase (see Fig. 3: AMP STROBE at t1 and t2 is low, the signals 20 corresponding to node 26 and 22 corresponding to node 24 are at Vdd), and wherein the nodes are set to a finalized state during the evaluate phase (see Fig. 3: AMP STROBE at t3 is high indicating the evaluate phase and signals 20 corresponding

to node 26 and 22 corresponding to node 24 are set to final states; see column 5, lines 18-36).

8. **Claims 1-5, 9-11, 13-15, 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Allmon (U.S. Patent 6,201,418).**

Regarding independent claim 1, Allmon discloses a method, comprising:

assigning a plurality of nodes (see Fig. 1: 12, 14) within a storage circuit to a predetermined state (see column 3, lines 64-67);

evaluating a plurality of signals coupled to the storage circuit (see column 3, lines 4-6), wherein evaluating the plurality of signals enables a first node (Fig. 1: 14) to change from its predetermined state (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage, IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage) and enables a second node to be more susceptible to perturbations (see column 3, lines 4-6, 34-37, 48-55); and

maintaining the second node (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34) in its predetermined state for a predetermined period of time, wherein maintaining the predetermined state reduces the storage circuit's susceptibility to soft errors (see e.g., column 3, lines 48-55 and column 4, lines 15-24).

Regarding dependent claim 2, Allmon discloses disabling a clock signal (Fig. 1: CLK) within the plurality of signals during a pre-charge phase (see column 2, lines 64-67).

Regarding dependent claim 3, Allmon discloses configuring an input signal within the plurality of signals during the pre-charge phase of the clock signal (see Fig. 1: CLK; column 2, lines 64-67).

Regarding dependent claim 4, Allmon shows enabling a clock signal during an evaluate phase (see Fig. 1: CLK; column 3, lines 4-6)

Regarding dependent claim 5, Allmon shows relating the predetermined period of time to the beginning of the evaluate phase of the clock signal (see Fig. 1: CLK; column 3, lines 4-6).

Regarding dependent claim 9, Allmon shows maintaining the second node (Fig. 1: 12) at their predetermined states using active pull-up techniques (see Fig. 1: P3 to Vdd).

Regarding independent claim 10, Allmon shows a storage circuit (Fig. 1) comprising:

a plurality of nodes including a first node (Fig. 1: 14) and a second node (Fig. 1: 12), wherein the second node is coupled to the first node (see Fig. 1: 12 is coupled to 14 through P2 or P3);

a plurality of signals (Fig. 1: CLK, IN_L, IN_H) coupled to the storage circuit, wherein the signals enable a first node to change from a predetermined state (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage,

IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage); and

a circuit element (Fig. 1: P3) coupled to the second node (Fig. 1: 12), wherein the circuit element maintains the second node in its predetermined state for a predetermined period of time (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34).

Regarding dependent claim 11, Allmon shows the circuit element further comprises metal oxide semiconductor field effect transistors (see Fig. 1: N1...N7, P1...P7).

Regarding dependent claim 13, Allmon shows an inverter (Fig. 1: P3, N3 is an inverter) is coupled between the first node and the second node.

Regarding dependent claim 14, Allmon shows a plurality of inverters (Fig. 1: P3 and N3 is an inverter as is P2 and N2) coupled between the first and second nodes.

Regarding dependent claim 15, Allmon shows the timing signal (Fig. 1: CLK) comprises a pre-charge phase (see column 2, lines 64-67).and an evaluate phase (see column 3, lines 4-6), and wherein the nodes are set high during the pre-charge phase (see column 2, lines 64-67), and wherein the nodes are set to a finalized state during the evaluate phase (see column 3, lines 34-37).

Regarding independent claim 20, Allmon shows a storage circuit (Fig. 1), comprising:

a means for enabling and disabling a clock signal (Fig. 1: CLK), wherein the means for enabling and disabling enables a plurality of nodes in the storage circuit to be

assigned a predetermined state (see column 2, lines 64-67) and wherein the means for enabling and disabling enables a first node (Fig. 1: 14) within the plurality of nodes to change states (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage, IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage); and

a means for maintaining a second node (Fig. 1: 12) within the plurality of nodes at a predetermined state while the first node is changing states, wherein the means for maintaining the second node at a predetermined state (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34) reduces the storage circuit's susceptibility to soft errors (see e.g., column 3, lines 48-55 and column 4, lines 15-24).

Regarding dependent claim 21, Allmon shows means for configuring an input signal (Fig. 1: IN_L, IN_H) and a clock signal (Fig. 1: CLK).

Regarding dependent claim 22, Allmon shows the clock signal (Fig. 1: CLK) comprises a pre-charge phase (column 2, lines 64-67) and an evaluate phase (column 3, lines 4-6) and the input signal (Fig. 1: IN_L, IN_H) is configured during the pre-charge phase and the first node changes states during the evaluate phase (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage, IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage) and the second node is maintained at its predetermined state during the evaluate phase (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 6-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allmon (U.S. Patent 6,201,418) as applied to claim 1 and claims 10-11, respectively, and further in view of Bansal (U.S. Patent 5,504,703).**

Regarding dependent claim 6, Allmon teaches the limitations discussed above in claim 1.

Allmon is silent with respect to a plurality of inverters between the first and second nodes.

Bansal teaches a plurality of inverters to delay signal propagation between the first and second nodes of a latch (see 3: INV1, INV2 between nodes 1 and 2; and INV3, INV4 between nodes 2 and 1) to reduce the effects of an ion strike, or single event upset (see column 3, line 35) on a node before it reaches the transistors controlling the other node (see e.g., column 3, lines 56-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Bansal to the teachings of Allmon such that additional inverters are placed between the first and second node to delay a signal

propagation for the purposes of reducing the effects of an ion strike on a node (see e.g., Bansal column 3, lines 56-60).

Regarding dependent claim 7, Allmon teaches the limitations discussed above in claim 1.

Allmon is silent with respect to maintaining the second node at its predetermined state using a plurality of transistors.

Bansal teach maintaining a second node (see Fig. 3: node 4) at its predetermined state using a plurality of transistors (see Fig. 3: T3 and INV3, INV4 with respect to Fig. 4: Tp connected to Vdd and Tn connected to ground; when node 3 is low, the PMOS T3 turns on and places Vdd on node2 which turns on the NMOS of INV3 to ground its output which turns on PMOS of INV4 which places and maintains Vdd on node4, the second node).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Bansal to the teachings of Allmon such that additional inverters, including a plurality of transistors to maintain the second node at a predetermined state, are placed between the first and second node to delay the signal propagated between the nodes for the purposes of reducing the effects of an ion strike on a node (see e.g., Bansal column 3, lines 56-60).

Regarding dependent claim 8, Bansal further shows the plurality of transistors (Fig. 3: T3 and INV4 with respect to Fig. 4: Tp) couple to the second node (see Fig. 3: node4) and also couple to a voltage source (Fig. 3, 4: Vdd).

Regarding dependent claim 12, Allmon teaches the limitations discussed above in claim 10 and 11 (from which this claim depends).

Allmon is silent with respect to varying the size of the transistors to vary the period of time that the second node is maintained in the predetermined state.

Bansal teaches varying the size of the channel of the transistors (Fig. 4: Tp and Tn) which make the inverters (Fig. 3: INV1…INV4) used to delay the signal between the first node (e.g., Fig. 3: node1) and the second node (e.g., Fig. 3: node 2) for the purpose of provide a desired delay and permit a needed level of single event upset (SEU) immunity (see column 3, lines 33-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Bansal to the teachings of Allmon such that additional inverters, including a plurality of transistors which have varied sizes (e.g., varied channel lengths and widths), are placed between the first and second node for the purposes of proving a desired delay between nodes which permits reducing the effects of an ion strike on a node (see e.g., Bansal column 3, lines 33-35 and 56-60).

11. **Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allmon (U.S. Patent 6,201,418).**

Regarding independent claim 16, Allmon teaches a sense amplifier comprising:

a plurality of nodes (Fig. 1: 12,14);

a timing signal (Fig. 1: CLK); and

at least one control signal (Fig. 1: IN_H, IN_L);

wherein the timing signal and the control signals cause a first node (Fig. 1: 14) within the plurality to change from an initialized state to a finalized state (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage, IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage) while a second node (Fig. 1: 12) within the plurality is maintained in an initialized state (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34); and

wherein maintaining the second node (Fig. 1: 12) while the first node (Fig. 1: 14) is changing reduces the storage circuit's susceptibility to soft errors (see e.g., column 3, lines 48-55 and column 4, lines 15-24).

Allmon is silent with respect to a computer system with a processor and system memory.

However, it is well-known in the art to use a sense amplifier in a memory as a data read-out means for the memory. And, it is further well-known to include a memory in a computer system with a processor as the temporary data storage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the Allmon sense-amplifier into a computer system including a processor and a memory for the purposes of providing a prior art sense amplifier to a computer system which would be well-recognized in the art to use a sense amplifier as the read-out means.

Regarding dependent claim 17, Allmon further teaches the timing signal (Fig. 1: CLK) comprises a pre-charge phase (see column 2, lines 64-67).and an evaluate phase (see column 3, lines 4-6).

Regarding dependent claim 18, Allmon further teaches the first and second nodes (Fig. 1: 14, 12) are initialized during the pre-charge phase (see column 2, lines 64-67), and the first node (Fig. 14) is changed from the initialized state to a second state during the evaluate phase (see column 3, lines 11-13, 19-20: one transistor, 24, which receives the higher input voltage, IN_H, turns on and grounds the corresponding pre-output node, 14 corresponding to 24, which was previously pre-charged to a high voltage), and wherein the second node (Fig. 1: 12) is maintained in the initialized state for at least a portion of the evaluate phase (see e.g., Fig. 1: 12; see Fig. 1: P3 puts VDD on 12 when 14 is Vss; see column 3, lines 23-34).

Regarding dependent claim 19, Allmon further teaches the at least one signal is configured during the pre-charge phase (see Fig. 1: CLK; column 2, lines 64-67).

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Zhang (U.S. Patent 6,026,011), Mehta et al. (U.S. Patent 6,222,404), Bailey (U.S. Patent 6,367,025), and Bailey et al. (U.S. Patent 6,400,186).

Zhang shows a latch storing the same data at two nodes with soft error immunity.

Mehta et al. show a dynamic flip-flop with isolation.

Bailey and Bailey et al. show a flip-flop differential sense amplifier.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/VanThu Nguyen/
Primary Examiner, Art Unit 2824